

SELF-TEST FOR LEAKAGE CURRENT OF DRIVER/RECEIVER STAGES

Abstract of the Disclosure

The present invention relates to a test for current leakage of driver/receiver stages, and in particular for bi-directional input/output stages (10) of a semiconductor chip. Two dedicated support transistor devices (56,58) are added into the prior art switching scheme, together with a simple control logic (48,50,52,60,62,64) for selectively controlling the two dedicated support transistor devices according to a predetermined test scheme. An on-chip self-test feature provides valid voltage levels which are convertible by the receiver (24) to predictable logic states at the evaluation line RDATA. The test can be performed autonomously on the chip without the requirement for an external test device.

Figures

Figure 1: A line graph showing the relationship between the number of hours spent studying and the score on a test. The x-axis represents 'Hours Studied' (0 to 10) and the y-axis represents 'Test Score' (0 to 100). The data points are as follows:

Hours Studied	Test Score
0	55
1	60
2	65
3	70
4	75
5	80
6	85
7	90
8	95
9	100
10	100

The graph shows a positive correlation between study hours and test scores, with the score increasing from 55 at 0 hours to 100 at 10 hours.